10-02-00

A

Please type a plus sign (+) inside this box [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b))

Attorney Docket No. 042390.P9724 Total Pages 2

First Named Inventor or Application Identifier Xia Dai

Express Mail Label No. EL627466574US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 21)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 5)

4. X Oath or Declaration (Total Pages 5)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. ___ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ___ Computer Readable Copy
b. ___ Paper Copy (identical to computer copy)
c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ___ Assignment Papers (cover sheet & documents(s))
9. ___ a. 37 CFR 3.73(b) Statement (where there is an assignee)
___X___ b. Power of Attorney
10. ___ English Translation Document (if applicable)
11. ___ a. Information Disclosure Statement (IDS)/PTO-1449
___ b. Copies of IDS Citations
12. ___ Preliminary Amendment
13. ___X___ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. ___ a. Small Entity Statement(s)
___ b. Statement filed in prior application, Status still proper and desired
15. ___ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ___ Divisional ___ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

___ Customer Number or Bar Code Label _____ (Insert Customer No. or Attach Bar Code Label here)

or

___X___ Correspondence Address Below

NAME John Patrick Ward, Reg. No. 40,216

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT ($) **$1134.00**

Complete if Known:
Application No. Not Yet Assigned
Filing Date Herewith
First Named Inventor Xia Dai
Group Art Unit Not Yet Assigned
Examiner Name Not Yet Assigned
Attorney Docket No. 042390.P9724

METHOD OF PAYMENT (check one)

1. [X] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

Deposit Account Number 02-2666
Deposit Account Name ______

[X] **Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17**

2. X **Payment Enclosed:**
X **Check**
___ **Money Order**
___ **Other**

FEE CALCULATION

1. **BASIC FILING FEE**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility application filing fee	690.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 690.00

2. **EXTRA CLAIM FEES**

			Extra Claims		Fee from below		Fee Paid
Total Claims	36	– 20** =	16	X	18	=	288.00
Independent Claims	5	– 3** =	2	X	78	=	156.00
Multiple Dependent						=	

****Or number previously paid, if greater; For Reissues, see below.**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 444.00

Patent fees are subject to annual revisions. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid.
See Forms PTO/SB/09-12

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	
Other fee (specify)					
Other fee (specify)					

SUBTOTAL (3) $ 0

*Reduced by Basic Filing Fee Paid

SUBMITTED BY:

Typed or Printed Name: John Patrick Ward, Esq.

Signature _____ Date September 30, 2000

Reg. Number 40,216 Deposit Account User ID _____ (complete if applicable)

Attorney Docket: 42390.P9724 *PATENT*

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS TO ENHANCE PROCESSOR POWER MANAGEMENT

INVENTORS:

XIA DAI

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026

(408) 720-8300

METHOD AND APPARATUS TO ENHANCE PROCESSOR POWER MANAGEMENT

FIELD OF THE INVENTION

The present invention relates to processors including microprocessors. Specifically, this invention relates to managing processor latency.

BACKGROUND OF THE INVENTION

Portable systems, such as portable computers, have become increasingly popular as replacements for desktop systems. A portable system relies on a battery as its power source when it is not connected to an external power source, such as an AC outlet. As battery life is limited, power consumption in the system is reduced typically by lowering the core supply voltage and the core clock frequency of the processor. Thus, the portable system operates in a high performance state when it is powered by an external source and in a low power state when powered by a battery.

In some portable systems, the transition between the two states occurs statically, for example, at reset or reboot. The Geyserville™ processor technology of the Intel Corporation, on the other hand, is capable of dynamically transitioning between the two states, i.e., without a processor reset. The Geyserville technology is an improvement over the technology that changes the performance states statically because it achieves the transitions seamlessly and relatively rapidly without user intervention.

Even the dynamic Geyserville technology, however, may take more than 500 micro seconds to adjust the core supply voltage and the core clock frequency of the processor. This latency is the result of the processor being placed in the deep sleep mode (ACPI Specification C3 mode) during the entire transition. ACPI Specification stands for the Advanced Configuration and Power Interface Specification, Revision 2.0, published on July 27, 2000. Additional latency results to re-activate the system clock input to the processor to enable it to exit deep sleep following the transition.

The high processor latency associated with Geyserville is undesirable because it is wasted time that slows down the system operation.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

Fig. 1 is a transition graph pertaining to the one embodiment.

Fig. 2 is a block diagram of a system according to one embodiment.

Fig. 3 is a block diagram of a power management control logic in the system of Fig. 2.

Fig. 4 is a flow diagram of a power management module according to one embodiment.

Fig. 5 is a flow diagram of a power management module according to another embodiment.

DETAILED DESCRIPTION

The present invention improves the Geyserville technology by reducing the processor latency associate with Geyserville. Power dissipation of the processor is proportional to core clock frequency and to the square of core supply voltage. As the core clock frequency is reduced, the minimum required core supply voltage level is also reduced, thereby dramatically reducing the processor's power consumption. Depending on the power consumption desired of the system, the system may be set at one of the multiple performance states. For example, if the system is only powered by battery (such as, when the system is being used as a portable unit remotely without access to an external power supply), the system is placed in a low power state to conserve power. However, if the system is powered by an external power source (such as, an alternating current or AC outlet), the system is placed in a high performance state.

In this description, the system may be a portable computer, a notebook computer, a hand-held electronic device, and the like. Also, the terms core clock frequency and processor clock frequency are synonymous. Also, the terms core supply voltage and processor supply voltage are synonymous. Additionally, the ensuing description refers to two performance states, low power and high performance, between which the transitions are performed.

Fig. 1 shows a transition graph to transition between the two states. In one embodiment, the transition, which may be performed by a controller formed of one or more layers (including, for example, software, firmware, and hardware), is performed in two different phases. In phase one, the core supply voltage level is adjusted. In phase two, the core clock frequency level is adjusted.

During the low power to high performance transition, phase two follows phase one. The core supply voltage level is elevated first such that it

is at least the minimum voltage level required to support the elevated core clock frequency level of phase two.

During phase one, the processor remains in the active mode (for example, ACPI Specification C0 mode) because the processor can continue to perform its functions properly at the elevated core supply voltage level

Performing phase 1 while the processor is in the active mode is one key feature of the present invention because that reduces the processor latency associated with Geyserville.

During phase 2, the processor is placed in the sleep mode. In one embodiment, the sleep mode is not any of the C0-C3 modes of the ACPI Specification. The sleep mode is not visible to the end user. During the sleep mode the core clock (for example, the phase locked loop circuit) and the system clock (which is an input to the processor) remain active but the processor typically performs no logical functions.

To the end user the processor seems to be in the deep sleep (C3) mode because it refuses to process requests from other system components. When viewed from inside the processor, however, the processor seems to be in the quick start (for example, ACPI Specification C2) mode because the core clock remains active and the system clock input to the processor remains active.

Performing phase 2 while the processor is in the sleep mode is another key feature of the present invention. Performing phase 2 in the sleep mode instead of the deep sleep mode (C3) reduces the latency to re-activate the system clock input to the processor after completing phase 2. In one embodiment of the present invention, phase 2 is performed in less than 5 microseconds.

In one embodiment of the present invention, the entire transition from low power to high performance is performed with less than 5 microseconds of latency.

During the high performance to low power transition, phase 1 follows phase 2. The processor clock frequency is reduced first such that when the processor supply voltage level is reduced later on during phase 1, the reduced processor core voltage level is adequate to support it. Phase 2 is performed in the same manner as with regards to the low power to high performance transition, except that the core frequency level is reduced instead of elevated. Phase 1 is also performed in the same manner as with regards to the low power to high performance transition, except that the core voltage level is reduced instead of elevated.

Both of the above performance states transitions are achieved seamlessly, relatively rapidly and dynamically without user intervention. It is contemplated that although this description refers specifically to a processor, other components in which performance states may be adjusted can be substituted in its place. Examples of such components are an application-specific integrated circuit (ASIC), a programmable gate array (PGA), a graphics subsystem, memory subsystem, buses or other discrete integrated devices.

Referring to Fig. 2, an example system 10 according to an embodiment of the invention includes a processor 12 that receives an external clock BCLK (from a clock generator 50) and a supply voltage (from a voltage regulator 52). The voltage regulator 52 and the clock generator 50 are both controllable to adjust the core supply voltage levels as well as the core clock frequencies in the processor 12, as further described below.

The main power supply voltages in the system 10 are provided by a power supply circuit 56 that is coupled to a battery 60 or an external power source outlet 58. When the external power source (not shown) is plugged into or removed from the external outlet source 58, an interrupt (e.g., a system management interrupt or SMI) may be generated to notify system software of the external power source insertion or removal. In addition,

docking the system 10 to a docking base unit may also indicate a power source transition. In one embodiment, a device driver may detect power source transitions and docking events by registering with the operating system for power and plug-and-play notifications, for example. Thus, depending on whether the system 10 is powered by an internal power source (e.g., battery 60) or by an external power source (e.g., as coupled through the external source outlet 58), the system 10 may be set at a suitable performance state. For example, when the external power source is coupled, the system 10 may operate in the high performance state; however, if the internal power source is coupled instead, the system 10 may operate at the low power state.

Additionally, the computer system 10 may provide a graphical user interface through which a user may specify the desired performance state of the system.

The processor 12 may be coupled to a cache memory 14 as well as to a host bridge 18 that includes a memory controller for controlling system memory 16. The host bridge 18 is further coupled to a system bus 22, which may in one embodiment be a Peripheral Component Interconnect (PCI) bus, as defined in the PCI Local Bus Specification, Production Version, Rev. 2.1, published on June 1, 1995. The system bus 22 may also be coupled to other components, including a video controller 24 coupled to a display 26 and peripheral slots 28.

A secondary or expansion bus 46 may be coupled by a system bridge 34 to the system bus 22. The system bridge 34 includes interface circuits to different ports, including a universal serial bus (USB) port 36 (as described in the Universal Serial Bus Specification, Revision 1.0, published in Jan. 1996) and ports that may be coupled to mass storage devices such as a hard disk drive, compact disc (CD) or digital video disc (DVD) drives, and the like.

Other components that may be coupled to the secondary bus 46 include an input/output (I/O) circuit 40 coupled to a parallel port, serial port, floppy drive, and infrared port. A non-volatile memory 32 for storing basic input/output system (BIOS) routines may be located on the bus 46, as may a keyboard device 42 and an audio control device 44, as examples. It is to be understood, however, that all components in the system 10 are for illustrative purposes and the invention is not limited in scope to the illustrated system.

Various software or firmware layers (formed of modules or routines, for example), including applications, operating system modules, device drivers, BIOS modules, and interrupt handlers, may be stored in one or more storage media in the system. The storage media includes the hard disk drive, CD or DVD drive, floppy drive, non-volatile memory, and system memory. The modules, routines, or other layers stored in the storage media contain instructions that when executed causes the system 10 to perform programmed acts.

The software or firmware layers can be loaded into the system 10 in one of many different ways. For example, code segments stored on floppy disks, CD or DVD media, the hard disk, or transported through a network interface card, modem, or other interface mechanism may be loaded into the system 10 and executed as corresponding software or firmware layers. In the loading or transport process, data signals that are embodied as carrier waves (transmitted over telephone lines, network lines, wireless links, cables, and the like) may communicate the code segments to the system 10.

In the description that follows, reference is made to specific signals and circuitry as well as to sequences of events--it is to be understood that the invention is not limited in scope to the illustrated embodiments.

Referring to Fig. 3, power management control logic according to an embodiment of the invention to control the core clock frequency and the

core supply voltage level is shown. In the illustrated embodiment, the control logic may be separated into a first portion 100 and a second portion 102. However, it is contemplated that the control logic may also be integrated in one component. The first control logic portion 100 may be included in the host bridge 18, and the second control logic portion 102 may be included in the system bridge 34. Alternatively the first and second control logic portions may be implemented as separate chips. In addition, instead of being configured with host and system bridges 18 and 34 as illustrated in Fig. 2, the circuitry may be implemented as a memory hub (including interfaces to the processor and system memory) and an input/output (I/O) hub (including interfaces to the system bus and secondary bus). In this other configuration, the control logic 100 and 102 may be implemented in the memory hub. With the memory and I/O hubs, messages rather than signals may be used to provide the same functionality as the control logic 100, 102. Alternatively, a serial link may be used for communication with the voltage regulator 52 and clock generator 50.

The power management control logic (100, 102) provides control signals to the voltage regulator 52 to adjust its supply voltage level and to the processor 12 to adjust the core clock frequency. In addition, the power management control logic (100, 102) is responsible for placing the processor 12 into the sleep mode to complete phase 2 of the transition sequence.

In one embodiment, the processor 12 includes a clock generator, which is a phase locked loop (PLL) circuit. The PLL circuit frequency may be varied according to the algorithm by storing data in a register. In one embodiment, the data is the bus ratio. The bus ratio is the ratio between the frequencies of the PLL circuit clock and the system clock BCLK. In one embodiment, the frequency of the system clock can remain the same while the PLL circuit clock frequency is changed. In further embodiments, the bus

ratios settings may be stored in programmable devices in the processor, including, for example, fuse banks or non-volatile memory.

A brief description of the interface signals between the power management control logic (100, 102) and the other components of the system follows. A signal VR_LO/HI# is provided by the control logic portion 100 to indicate to the voltage regulator 52 the required core supply voltage.

A signal LO/HI# provided by the control logic portion 100 to the processor 12 determines whether the core clock frequency is to be set to a high or low level. As an example, the core clock frequency may be either 350 MHZ or 450 MHZ depending on whether LO/HI# is active or not. It is noted that additional signals may be used to adjust the core clock frequency to more than two levels. Similarly, additional signals other than VR_LO/HI# may also be used to control the voltage supply levels provided by the voltage regulator 52. In the illustrated embodiment, a signal G_LO/HI# from the system bridge 34 indicates the desired system state and controls the states of LO/HI# and VR_LO/HI#. Additional signals may be used to define more than two system states.

According to one embodiment of the invention, when the voltage regulator on signal (VR_ON) is active (which is true whenever the system is on), the voltage regulator 52 settles to the output selected by VR_LO/HI# (a low level or a high level). By way of example, a low supply voltage level may be about 1.3 V while a high supply voltage level may be about 1.8 V.

Fig. 4 illustrates a flow diagram of a power management module utilizing the power management control logic of Fig. 3 to perform low power to high performance dynamic performance state transition, in the system 10 of Fig. 2. The power management module may be implemented as a software module, in system firmware (e.g., system bios or SMI handler), as part of the operating system, as a device driver, or as a combination of the above. The power management module determines (at E1) that the system

which was originally battery operated has now been plugged into the AC outlet. Next, the power management module indicates to switch up the performance state level of the processor. This may be performed, for example, by writing a predefined value to a register to indicate the new performance state level of the processor 12. The controlled register may be defined in memory or I/O address space. In addition, programming of the register may be defined under the ACPI specification.

Thus, in one embodiment, one or more ACPI objects may be created to indicate to the operating system that the system 10 is capable of transitioning between the two performance states and to demand those resources when the system is ready to perform the transitions. The location and structure of the controlled register may be defined under an ACPI object. Furthermore, one or more ACPI objects may define the core clock frequencies and supply core voltage levels to be used in each performance state, the expected power consumption in each performance state, and other information.

Next, the power management module requests the input output control hub (ICH) to prepare for and assist in the performance state transition (at E2). Next, the control logic 100 indicates to the voltage regulator 52 that the voltage regulator 52 output should be at the high performance state core supply voltage level. In one embodiment, the voltage regulator 52 includes the Geyserville Application Specific Integrated Circuit (GASIC) to elevate the voltage regulator 52 output with a controlled ramping rate in a 25MV-50MV step wise fashion (at E3). GASIC elevates the voltage regulator 52 output in accordance with a VID voltage level table. The high performance state core supply voltage is established when the voltage regulator 52 output reaches the peak voltage level stated in the VID table (at E4). Next, the power management module places the processor 12 into the quick start mode (C2) (at E5). Next, the power management module

informs the platform components that the processor can no more process their requests because it is about to enter into the sleep state (at E6). Next, the input output control hub (ICH) snoops to insure memory core coherency, for example, among the L1 cash, the L2 cash and the DRAM (at E7). Next, the power management module places the processor in the sleep state (at E8). Next, the power management adjusts the core clock frequency to the high performance level (at E9). In one embodiment, a phased locked loop (PLL) relocks to a new bus ratio. Next, the power management module removes the processor 12 from the sleep state (at E10). Finally, the power management module removes the processor from the quick start (C2) state (at E11).

Fig. 5 illustrates a flow diagram of a power management module utilizing the power management control logic of Fig. 3 to perform high performance to low power dynamic performance state transition, in the system 10 of Fig. 2. The power management module determines (at E21) that the system, which was originally plugged into an AC outlet, is now battery operated. Next, the power management module indicates to switch down the performance state level of the processor 12. Next, the power management module requests the input output control hub (ICH) to prepare for and assist in the performance state transition (at E22). Next, the power management module places the processor 12 into the quick start mode (C2) (at E23). Next, the power management module informs the platform components that the processor can no more process their requests because it is about to enter into the sleep state (at E24). Next, the input output control hub (ICH) snoops to insure memory coherency, for example, among the L1 cash, the L2 cash and the DRAM (at E25). Next, the power management module places the processor in the sleep state (at E26). Next, the power management adjusts the core clock frequency to the low power level (at E27). In one embodiment, a phased locked loop (PLL) relocks to a new bus

ratio. Next, the power management module removes the processor 12 from the sleep state (at E28). Next, the power management module removes the processor from the quick start (C2) state (at E29). Next, the control logic 100 indicates to the voltage regulator 52 that the voltage regulator 52 output should be at the low power state core supply voltage level. In one embodiment, the voltage regulator 52 includes the Geyserville Application Specific Integrated Circuit (GASIC) to reduce the voltage regulator 52 output with a controlled rate in a 25MV-50MV step wise fashion (at E30). GASIC reduces the voltage regulator 52 output in accordance with a VID voltage level table. The low power state core supply voltage is established when the voltage regulator 52 output reaches the bottom voltage level stated in the VID table (at E31).

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

In addition, the methods as described above can be stored in memory of a computer system as a set of instructions to be executed. In addition, the instructions to perform the methods as described above could alternatively be stored on other forms of computer-readable mediums, including magnetic and optical disks. For example, the method of the present invention can be stored on computer-readable mediums, such as magnetic disks or optical disks that are accessible via a disk drive (or computer-readable medium drive).

CLAIMS

What is claimed is:

1. A system comprising:

a component;

a detector to detect a power management event; and

a controller to transition, in response to the power management event, a first setting of the component from a first performance mode to a second performance mode,

the controller to transition the component to a reduced activity state, and to change a second setting of the component from a first performance mode to a second performance mode.

2. The system of claim 1, wherein the component is the processor.

3. The system of claim 1, wherein changing the first setting of the component includes changing the core processor supply voltage level from a first voltage level to a second, higher voltage level.

4. The system of claim 1, wherein the reduced activity state includes the sleep state.

5. The system of claim 1, wherein changing the second setting of the component includes changing the core processor clock frequency from a first frequency level to a second, higher frequency level.

6. The system of claim 1, wherein the core processor clock remains active during the sleep state.

7. The system of claim 1, wherein a system clock input to the processor remains active during the sleep state.

8. The system of claim 1, wherein the power management event includes a change of the system power source from an internal power source to an external power source.

9. The system of claim 1, wherein changing the first setting of the component can requires 500 microseconds.

10. The system of claim 1, wherein changing the second setting of the component requires less than 5 microseconds.

11. A system comprising:

a component;

a detector to detect a power management event;

a controller to transition the component, in response to the power management event, to a reduced activity state,

the controller to change a first setting of the component from a first performance mode to a second performance mode,

the controller to transition the component out of the reduced activity state, and to transition a second setting of the component from a first performance mode to a second performance mode.

12. The system of claim 11, wherein the component is the processor.

13. The system of claim 11, wherein the reduced activity state includes the sleep state.

14. The system of claim 11, wherein changing the first setting of the component includes changing the core processor clock frequency from a first frequency to a second, lower frequency.

15. The system of claim 11, wherein changing the second setting of the component includes changing the core processor supply voltage level from a first voltage level to a second, lower voltage level.

16. The system of claims 11, wherein a system clock input to the processor remains active during the sleep state.

17. The system of claims 11, wherein the core processor clock remains active during the sleep state.

18. The system of claim 11, wherein the power management event includes a change of the system power source from an external power source to an internal power source.

19. The system of claim 12, wherein changing the first setting of the component requires less than 5 microseconds.

20. The system of claim 11, wherein changing the second setting of the component can requires 500 microseconds.

21. A computer-readable medium having stored thereon a set of instructions to translate instructions, the set of instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event;

transitioning a first setting of a component from a first performance mode to a second performance mode in response to the power management event,

transitioning the component to a reduced activity state, and to change a second setting of the component from a first performance mode to a second performance mode,

if the power management event includes the system power source switching from an internal power source to an external power source; and

transitioning the controller to a reduced activity state in response to the power management event,

changing the second setting of the component from the second performance mode to the first performance mode,

transitioning the component out of the reduced activity state, and transitioning the second setting of the component from the second performance mode to the first performance mode,

if the power management event includes the system power source switching from an external power source to an internal power source.

22. The computer-readable medium of claim 21, wherein the first setting of the component includes the core processor supply voltage level.

23. The-computer readable medium of claim 21, wherein the component is the processor.

24. The computer-readable medium of claim 22, wherein the second performance mode includes a higher voltage level than the first performance mode.

25. The computer-readable medium of claim 21, wherein the reduced activity state includes the sleep state.

26. The computer-readable medium of claim 21, wherein the core processor clock remains active during the sleep state.

27. The computer-readable medium of claim 21, wherein the second setting of the component includes the core processor clock speed.

28. The computer-readable medium of claim 27, wherein the second performance mode includes a higher frequency level than the first performance mode.

29. The computer-readable medium of claim 21, wherein a system clock input to the processor remains active during the sleep state.

30. The computer-readable medium of claim 21, wherein changing the second setting of the component requires 500 microseconds.

31. An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller to transition, in response to the indication, transition a power supply voltage level of a component from a first level to a second, higher level,

the controller to transition the component to a low activity state, and to change a core component clock frequency from a first level to a second, higher level, while the component is in the low activity state.

32. The apparatus of claim 31, wherein core component clock and a system clock input to the component remain active during the low activity state.

33. The apparatus of claim 31, wherein the indication is generated in response to a change in a power source in the system from an internal power source to an external power source.

34. An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller to transition the component to a low activity state in response to the indication,

the controller to change the component core clock frequency from a first level to a second, lower level, while the component is in the low activity state,

the controller to transition the component out of the reduced activity state, and to transition a power supply voltage level of the component from a first level to a second, lower level.

35. The apparatus of claim 34, wherein the core component clock and a system clock input to the component remain active during the low activity state.

36. The apparatus of claim 34, wherein the indication is generated in response to a change in a power source in the system from an external power source to an internal power source.

ABSTRACT OF THE INVENTION

A method and an apparatus to dynamically transition a processor between two performance states, high performance and low power. Predetermined core clock frequency and supply voltage levels of the processor define each performance state. Transitioning the supply voltage while the processor is in the active mode and transitioning the frequency while the processor is in the sleep mode significantly reduce the processor latency.

Transition Graph

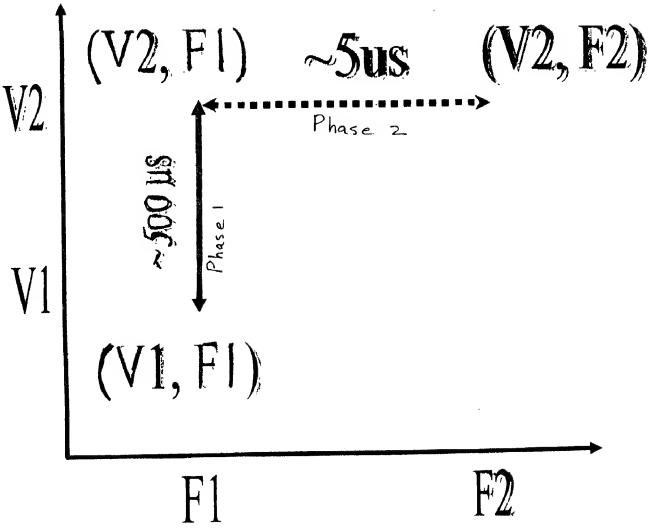

FIG.1

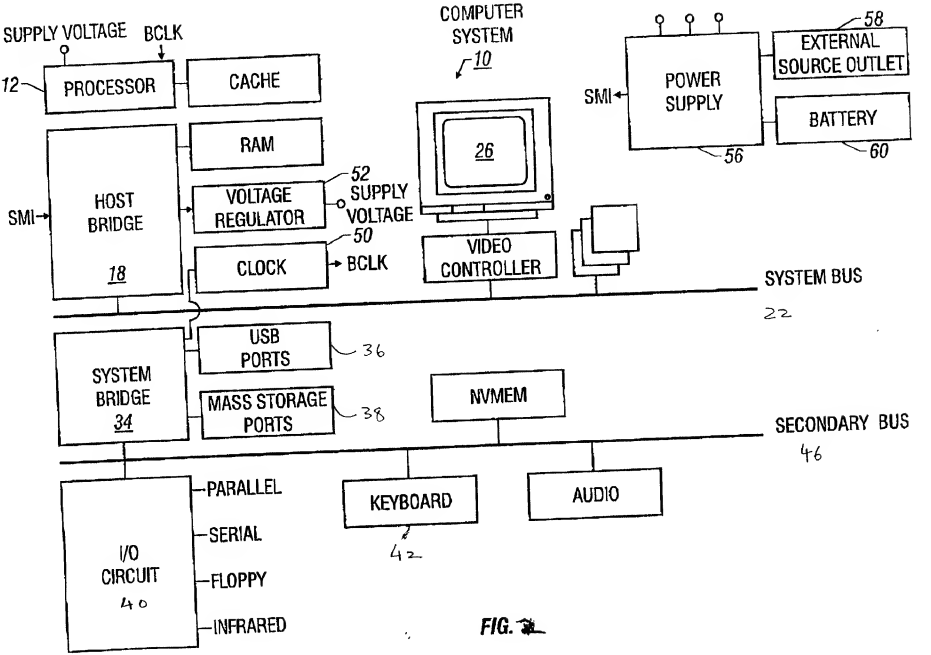

FIG. 1

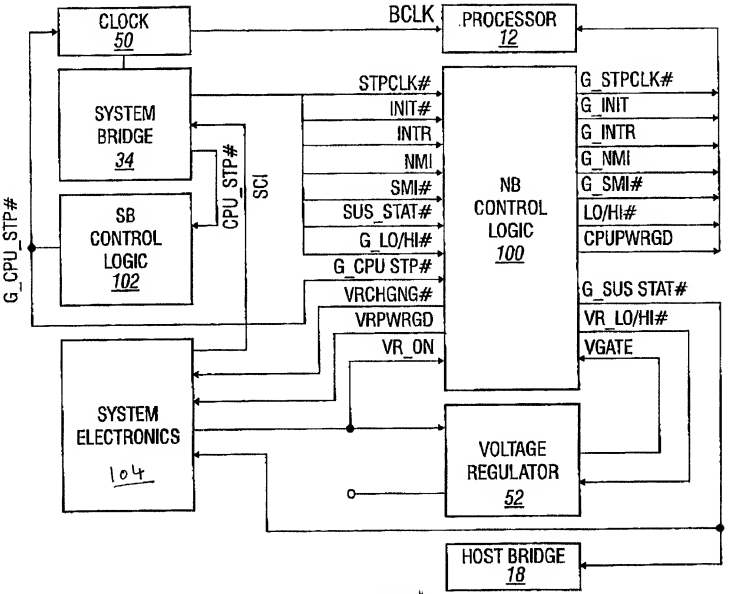

FIG. 3

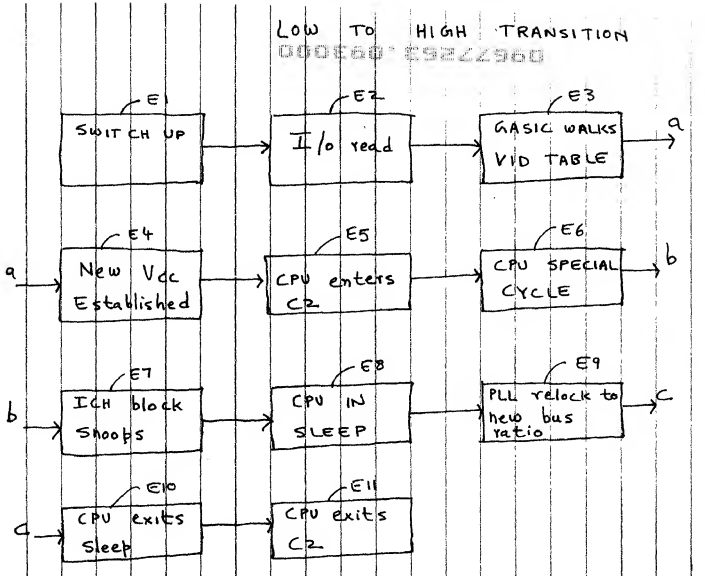
LOW TO HIGH TRANSITION
E1
SWITCH UP
E2
I/O read
E3
BASIC WALKS VID TABLE
a
E4
New Vcc Established
E5
CPU enters C2
E6
CPU SPECIAL CYCLE
b
E7
ICH block Snoops
E8
CPU IN SLEEP
E9
PLL relock to new bus ratio
c
E10
CPU exits Sleep
E11
CPU exits C2

FIG. 4

High to Low Transition

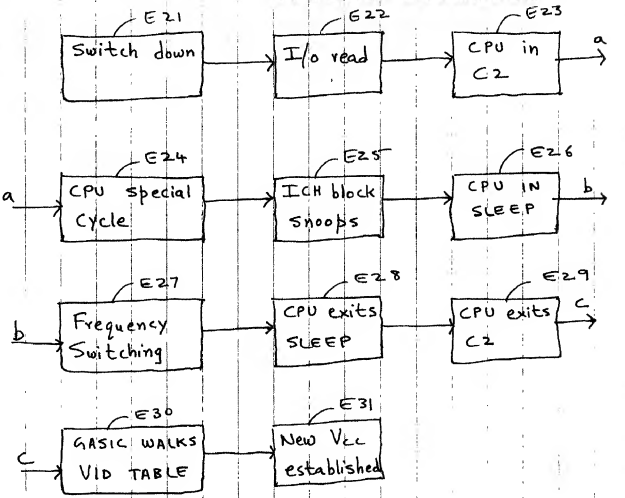

FIG. 5

Attorney's Docket No.: 042390.P9724 Patent

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
METHOD AND APPARATUS TO ENHANCE PROCESSOR POWER MANAGEMENT

the specification of which

_X_ is attached hereto.
___ was filed on (MM/DD/YYYY) _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on (MM/DD/YYYY) _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

(Application Number)	(Filing Date – MM/DD/YYYY)
(Application Number)	(Filing Date – MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	(Filing Date – MM/DD/YYYY)	(Status -- patented, pending, abandoned)
(Application Number)	(Filing Date – MM/DD/YYYY)	(Status -- patented, pending, abandoned)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to John P. Ward, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to John P. Ward, (408) 720-8300.

(Name of Attorney or Agent)

(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Xia Dai

Inventor's Signature ______________________ Date ______________

Residence ______________________ Citizenship ______________

(City, State) (Country)

Post Office Address ______________________

APPENDIX A

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Lisa N. Benado, Reg. No. 39,995; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Gregory D. Caldwell, Reg. No. 39,926; Andrew C. Chen, Reg. No. 43,544; Thomas M. Coester, Reg. No. 39,637; Donna Jo Coningsby, Reg. No. 41,684; Florin Corie, Reg. No. 46,244; Dennis M. deGuzman, Reg. No. 41,702; Stephen M. De Klerk, Reg. No. 46,503; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Sanjeet Dutta, Reg. No. 46,145; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; George Fountain, Reg. No. 37,374; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Libby N. Ho, Reg. No. 46,774; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Sang Hui Kim, Reg. No. 40,450; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; George Brian Leavell, Reg. No. 45,436; Kurt P. Leyendecker, Reg. No. 42,799; Gordon R. Lindeen III, Reg. No. 33,192; Jan Carol Little, Reg. No. 41,181; Robert G. Litts, Reg. No. 46,876; Joseph Lutz, Reg. No. 43,765; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Daniel E. Ovanezian, Reg. No. 41,236; Kenneth B. Paley, Reg. No. 38,989; Gregg A. Peacock, Reg. No. 45,001; Marina Portnova, Reg. No. 45,750; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; Joseph A. Twarowski, Reg. No. 42,191; Tom Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. 46,322; Thomas C. Webster, Reg. No. 46,154; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Firasat Ali, Reg. No. 45,715; Justin M. Dillon, Reg. No. 42,486; Thomas S. Ferrill, Reg. No. 42,532; and Raul Martinez, Reg. No. 46,904, my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.